

The diagram shows a two-port network  $A_1$ . The input port, labeled  $\underline{1}$ , is connected to a voltage source  $U_{in}$ . The output port, labeled  $\underline{2}$ , is connected to a load resistor  $R_{in}$ . The output voltage is  $U_{out}$ . The internal circuit of  $A_1$  contains a capacitor  $C$  in series with a resistor  $R$ . The current through the capacitor is  $I_u$ , and the current through the resistor is  $I_1$ . The output current is  $I_2$ . The output port is also labeled with  $21$  and  $22$ .

The diagram shows a two-port network. The input port is labeled  $R_{in}$  and the output port is labeled  $R_{out2}$ . The network consists of a resistor  $R$  in series with a parallel combination of a capacitor  $C$  and a resistor  $R$ . The capacitor  $C$  is labeled  $R_{out1}$ .

Fig. 3

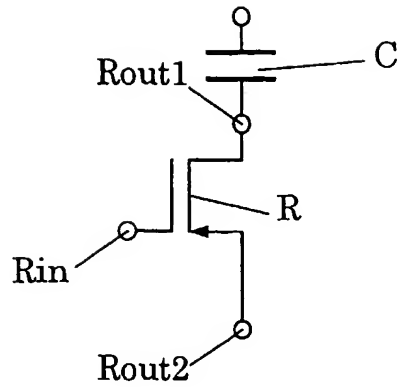


Fig. 4

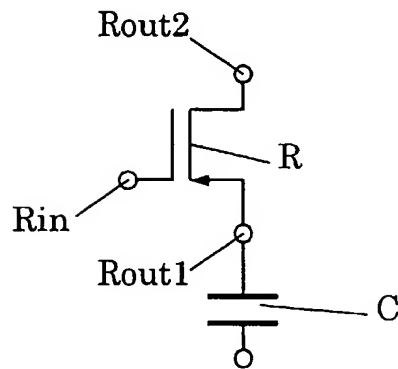
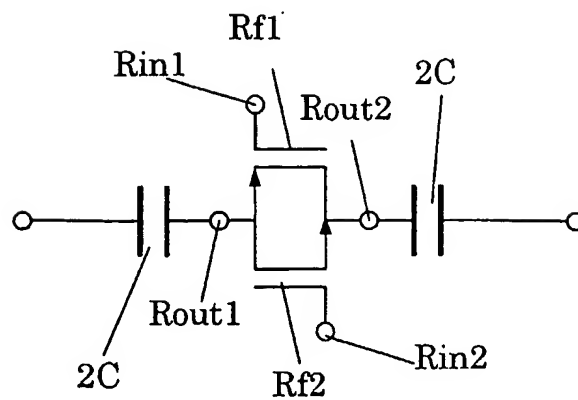


Fig. 5



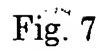


Fig. 8

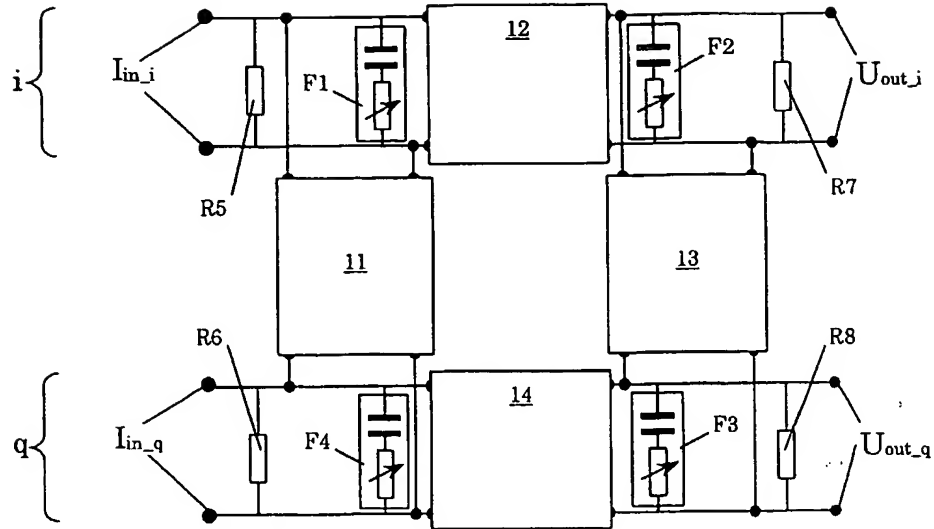


Fig. 9

